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ATE VISION 2020

3rd IEEE International Workshop on Automated Test Equipment: ATE Vision 2020

www.ATEVision.com

San Francisco Marriott Marquis,
San Francisco, California, USA
Thursday July 15, 2010

ATE Vision is the only dedicated IEEE workshop focused on examining where the ATE industry is heading in the near-term as well as in the long-term. The workshop won the IEEE/.TTTC most successful workshop award. Various technology and business trends pose significant challenges to the ATE industry. To meet those challenges the industry needs to innovate in areas beyond the traditional ATE box. The goal of this workshop is to create an informal forum to discuss those innovations relevant to ATE developers and users. Are our roadmaps addressing future test challenges? Are we investing our research dollars in the right areas? Do we have the right business models in place to succeed in the future? Join the discussion!

- Critical "future-proof" ATE capabilities
- Test methods for future defects
- 3D device testing ideas and techniques
- Power testing needs for Green technology
- Protocol Aware Techniques
- High-speed IO Test
- Ensuring test quality while minimizing test cost
- Ways to streamline our test efforts
- Killer ATE Products Ideas

Contact General Chair: Erik.Volkerink@Verigy.com

Session 1 - ATE Vision 2020 Opening

Time		
8:30am 8:35am		**Opening Remarks** *Erik Volkerink, General Chair*
8:35am 8:40am		**Opening Remarks** *Dave Armstrong, Program Chair*
8:40am 9:30am		**Keynote Address: ATE Countdown** *Ron Leckie, Infrastructure Advisors*
9:30am 10:00am		**Break**

Session 2 – Innovative Test Methodologies

Chair: Dave Armstrong, Advantest

Time		
10:00am 10:30am	1.1	**Closing the Structural/Functional Test Gap** *Han Ta, Cisco*
10:30am 11:00am	1.2	**Expanding test coverage at sort to reduce overall product cost** *Larry Levy, FormFactor*
11:00am 11:30am	1.3	**KGD Test and Challenges and solutions for TSV based devices** *Marc Loranger, FormFactor*
11:30am 12:00pm	1.4	**3D Test Challenges and Probing Concepts** *Stojan Kanev, Cascade Microtech*
12:00pm 1:00pm		**Lunch**

Session 3 - Test Requirements 2020 Panel

Moderator: Dan Hutcheson
VLSI Research

Time	
1:00pm 2:00pm	*Panelists:* *Pete Hodakievic, AMD* *Adam Wright, Altera* *Roger Barth, Micron* *Muru Yogathsan, StatsChipPac* *Andy Evans, Broadcom*
2:00pm 2:30pm	**Break**

Session 4 - Breakthroughs in Test Software

Chair: Ken Lanier, Teradyne

Time		
2:30pm 3:00pm	4.1	**Adaptive Test Today and + 20** *Robert Daasch, Portland State University*
3:00pm 3:30pm	4.2	**Beyond pass/fail test: The EDA perspective on the role of ATE** *Geir Eide, Mentor Graphics*
3:30pm 4:00pm		**Break**

Session 5 - Reducing Cost of Test

Chair: Ben Brown, LTX-Credence

Time		
4:00pm 4:30pm	5.1	**Towards a Universal Digital Pin Architecture: From DC to 10GHz+** *Mohamed Hafed, DFT Microsystems*
4:30pm 5:00pm	5.2	**Multi-system Architecture: A New Twist in Cost-of-Test Management** *Len Van Eck, LTX-Credence*
5:00pm 5:30pm	5.3	**Welcome (Back) To Functional Test** *Ken Lanier, Teradyne*
5:30pm 6:00pm		**Break**

Session 6: Test Solutions 2020 Panel

Moderator: Rick Nelson
Test & Measurement World

Time	
6:00pm 7:00pm	*Panelists:* *Gary Fleeman, Advantest* *Erik Volkerink, Verigy* *Jack O'Brien, Teradyne* *Steve Wigley, LTX-Credence* *Ben Eldridge, FormFactor*
7:00pm	**Open Mike & Adjourn**

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